Oak Technology
Incorporated

October 1991

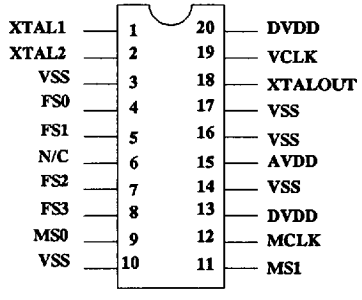
OTI-068 Dual Video/Memory Clock Generator

INTRODUCTION

The OTI-068 Dot Clock Generator is a dual phase frequency synthesizer capable of generating up to 16 video clock frequencies and 4 memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the OTI-068 provides a low power, small footprint, low cost solution to the generation of video dot clocks. Outputs are compatible with SVGA, VGA, EGA, MCGA, CGA, MDA, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Phase locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

FEATURES

- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystem.
- Improved pinout-easier board layout.
- Glitch-free frequency transitions.
- Provision for external frequency input.
- Internal clock remains locked when external frequency inputs are selected.
- Low power CMOS device technology.
- Small footprint-20 pin DIP or SO.
- Integral loop filter components.
- Supports VESA-standard high vertical refresh rates when used with OTI-067 or OTI-077 VGA controllers.
- Guaranteed performance up to 78 MHz.
- Advanced PLL for low phase-jitter.
- Frequency change detection circuitry enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information.
- Buffered XTAL out.



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Circuit and Application Options

The OTI-068 will typically derive its frequency reference from a series resonant crystal connected between pins 1 and 2. This signal may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts a 0.047 microfarad capacitor should be used to couple the reference signal into XTAL. Pin 2 must be left open.

Power Supply Conditioning

The OTI-068 is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the Vco, the ease of application has been substantially improved over the OTI-069 dot clock. If a stable and noise free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in figure. Figure 2 is the normal configuration for 5 volt only applications.

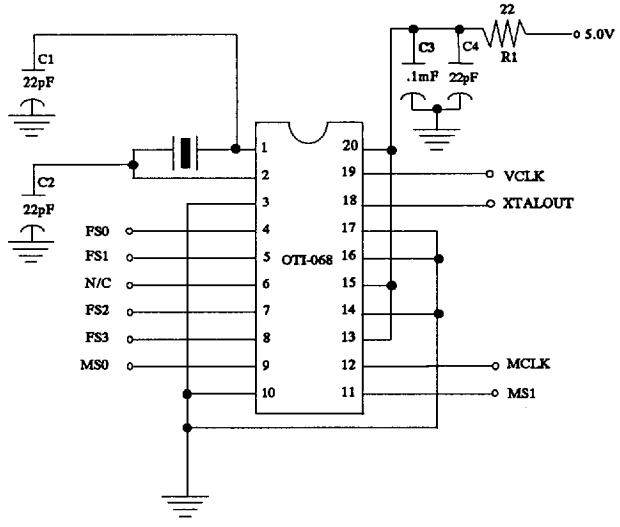


FIGURE 2

The number and differentiation of the analog and digital supply pin are intended for maximum performance products. In most applications, all Vdd's may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, the effect of packaging has been minimized. Using multiple pins has also minimized the interaction of the digital and analog supply currents.

Applications

Layout Considerations

Using the OTI-068 on video graphics adapter cards or on PS2 motherboards is straight-forward, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the OTI-068 do not use its ground. In applications using a multilayer board, Vss should be connected directly to the ground plane. Multiple pins are used for all analog and digital Vss and Vdd connections to permit extended frequency VCLK operation at 78 MHz. However, in all cases, all Vss and Vdd pins should be connected.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series resonant crystal should be connected between XTAL1(1) and XTAL2(2). In Oak Technology applications this will be a 14.31818 MHz crystal. Maintain short lead lengths between the crystal and the OTI-068. In some applications it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts it may be connected directly to XTAL(1). If the signal amplitude is less than 3.5 volts, connect the clock through a 0.047 microfarad capacitor to XTAL1(1), and keep the lead length of the capacitor to XTAL1(1) to a minimum to reduce noise susceptibility. This input is internally biased at Vdd/2 since TTL compatible clocks typically exhibit a Voh of 3.5V. Capacitively coupling the input restores noise immunity. The OTI-068 is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2(2) should be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the OTI-068 provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the XTALOUT(18) output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects VCLK(19) or MCLK(12) and other components in the system should be kept as short as possible. The OTI-068 outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the OTI-068. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase jitter as well as EMI.

Digital Inputs

FS0(4), FS1(5), FS2(7), FS3(8), are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. The internal power-on clear signal will force an initial frequency code corresponding to an all zeroes input state. MS0(9) and MS1(11) are the corresponding memory select inputs and are not strobbed.

SPECIFICATIONS

Absolute Maximum Ratings

Supply Voltage	Vdd		-0.5V to +7V
Input Voltage	Vin		-0.5V to VDD +0.5V
Output Voltage	Vout		-0.5V to VDD +0.5V
Clamp Diode Current	Vik & Iok		+/-30mA
Output Current Per Pin	Iout		+/-50mA
Operating Temperature	To		0° C to +70° C
Storage Temperature	Ts		-85° C to +150° C
Power Dissipation	Pd		500 mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that Vin and Vout be constrained to >= Vss and <=Vdd.

D.C. Characteristics (0^0C to 70^0C)

* The following inputs have pull-ups: FS0-3, MS0-1, STROBE.

Symbol	Parameter	Min	Max	Units	Conditions
Vdd	Operating Voltage Range	4	5.5	V	
Vil	Input Low Voltage	Vss	0.8	V	Vdd=5V
Vih	Input High Voltage	2	Vdd	V	Vdd=5V
Iih	Input Leakage Current	-	10	uA	Vin=Vcc
Vol	Output Low Voltage	-	0.4	V	Iol=4.0 mA
Voh	Output High Voltage	2.4	-	V	Ioh=4.0 mA
Idd	Supply Current	-	27	mA	Vdd=5V, VCLK= 80 MHz
Rup*	Internal Pullup Resistors	50	200	K Ohm	Vdd=5V, Vin=0V
Cin	Input Pin Capacitance	-	8	pF	Fc=1 MHz
Cout	Output Pin Capacitance	-	12	pF	Fc=1 MHz

AC Timing Characteristics

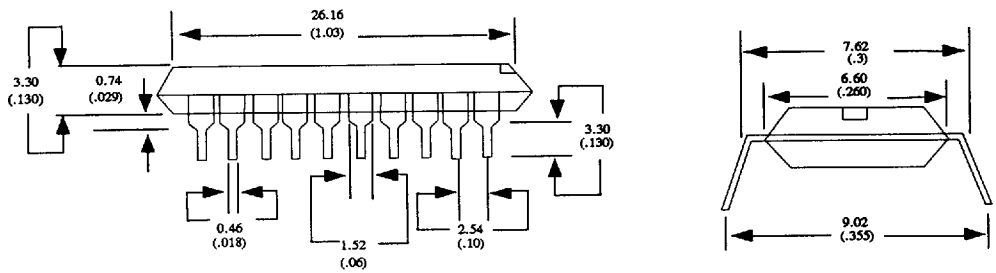
The following notes apply to all parameters presented in this section.

1. Xtal Frequency = 14.31818 MHz.
2. Tc = 1/Fc
3. All units are in nanoseconds (ns).
4. Rise and fall time between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0°C to 70°C

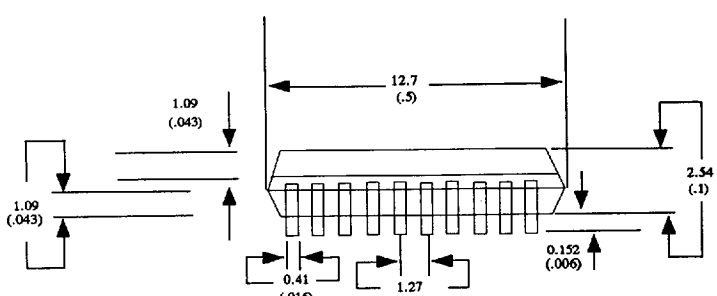
Symbol	Parameter		Min	Max	Notes
		Strobe Timing			
Tpw	Strobe Pulse Width		20	-	
Tsu	Setup Time Data to Strobe		10	-	
Thd	Hold Time Data to Strobe		10	-	
		MCLK and VCLK Timings			
Tr	Rise Time		-	3	Duty Cycle 40% min to
Tf	Fall Time		-	3	60% max
-	Frequency Error			0.5	%
-	Maximum Frequency			135	MHz
-	Propogation Delay for		-	15	ns
	Pass Through Frequency				

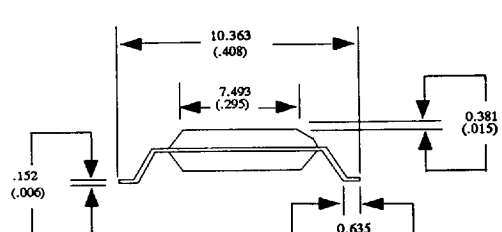
Package Dimensions

All Dimensions in mm (inches)



20 Pin DIP Package





20 Pin S.O. Package

FIGURE 3

OTI-068 Standard Frequencies

As shown in the table below, the OTI-068 requires four frequency select inputs (FS0-FS3) to determine which of the 16 clock frequencies available will be used. FS0-FS2 are controlled using the CSEL0-CSEL2 pins of the OTI VGA graphics controller being used. FS3 is controlled by a jumper or switch connected to pin 8 of the OTI-068. The memory clock speeds may be controlled by tying the inputs to MS0 and MS1 high or low depending on the desired frequency. They may also be controlled by a jumper or switch connected to pins 9 and 11 of the OTI-068.

Oak Standard Pixel Clock Table (FS3=0)

	FS3	FS2	FS1	FS0	Video Clock Address (HEX)	Frequency (MHz)
	0	0	0	0	0	25.175
	0	0	0	1	1	28.322
	0	0	1	0	2	65.000
	0	0	1	1	3	44.900
	0	1	0	0	4	28.322
	0	1	0	1	5	36.000
	0	1	1	0	6	40.000
	0	1	1	1	7	36.000

Oak High Vertical Refresh Table (FS3=1)

	FS3	FS2	FS1	FS0	Video Clock Address (HEX)	Frequency (MHz)
	1	0	0	0	8	25.175
	1	0	0	1	9	28.322
	1	0	1	0	A	78.000
	1	0	1	1	B	65.000
	1	1	0	0	C	63.000
	1	1	0	1	D	72.000
	1	1	1	0	E	40.000
	1	1	1	1	F	50.000

Memory Clock Table

			MS1	MS0	Memory Clock Address (HEX)	Frequency (MHz)
			0	0	0	44.000
			0	1	1	50.000
			1	0	2	66.000
			1	1	3	40.000

All patterns shown above use 14.31818 MHz as the input reference frequency.