STANDARD VGA REGISTERS

(Based on a document provided by Oak Technologies)

VGA REGISTERS INDEX

GENERAL

These registers control the overall activity of the VGA controller.

Register	R/W	Mono Port	Color Port	Index
Miscellaneous Output	W	3CC/3C2	3CC/3C2	
Input Status 0	R	3C2	3C2	
Input Status 1	R	3BA	3DA	
Feature Control	R/W	3CA/3BA	3CA/3DA	
DAC State	R	03C7	03C7	

SEQUENCER

The sequencer controls basic aspects of the clocks that feed into the VGA controller.

Register	R/W	Mono Port	Color Port	Index
Sequencer Address	R/W	3C4	3C4	
Reset	R/W	3C5	3C5	00
Clocking Mode	R/W	3C5	3C5	01
Plane Mask	R/W	3C5	3C5	02
Character Map Select	R/W	3C5	3C5	03
Memory Mode	R/W	3C5	3C5	04

GRAPHICS CONTROLLER

The graphics controller settings control how the system processor reads and writes to and from video memory.

Register	R/W	Mono Port	Color Port	Index
Graphics Controller Index	R/W	3CE	3CE	
Set/Reset	R/W	3CF	3CF	00
Enable Set/Reset	R/W	3CF	3CF	01
Color Compare	R/W	3CF	3CF	02
DataRotate	R/W	3CF	3CF	03

Read Map Select	R/W	3CF	3CF	04
Mode	R/W	3CF	3CF	06
Miscellaneous	R/W	3CF	3CF	06
Color Don't Care	R/W	3CF	3CF	07
Bit Mask	R/W	3CF	3CF	08

ATTRIBUTE CONTROLLER

These registers are the original CGA/EGA palette and border color registers. They are pretty much obsolete, except for text modes.

Register	R/W	Mono Port	Color Port	Inde:
Attribute Controller Index	R/W	3C0	3C0	
Color Palette Register 0-15	R/W	3C0	3C0	00-0
Mode Control	R/W	3C0	3C0	10
Overscan Control	R/W	3C0	3C0	11
Color Plane Enable	R/W	3C0	3C0	12
Horizontal Pixel Panning	R/W	3C0	3C0	13
Color Select	R/W	3C0	3C0	14

CRT CONTROLLER

This block of registers controls the various counters that are used to generate the video timing signals (VSYNC, HSYNC, BLANK, etc) and for clocking out video data.

Register	R/W	Mono Port	Color Port	Inde:
CRTC Address	R/W	3B4	3D4	
Horizontal Total	R/W	3B5	3B5	00
Horizontal Display Enable End	R/W	3B5	3D5	01
Start Horizontal Blanking	R/W	3B5	3D5	02
End Horizontal Blanking	R/W	3B5	3D5	03
Start Horizontal Retrace Pulse	R/W	3B5	3D5	04
End Horizontal Retrace	R/W	3B5	3D5	05
Vertical Total	R/W	3B5	3D5	06
Overflow	R/W	3B5	3D5	07
Preset Row Scan	R/W	3B5	3D5	08
Maximum Scan Line	R/W	3B5	3D5	09
Cursor Start	R/W	3B5	3D5	OA
Cursor End	R/W	3B5	3D5	OB
Start Address High	R/W	385	3D5	OC
Start Address Low	R/W	3B5	3D5	OD
Cursor Location High	R/W	3B5	3D5	OE

Cursor Location Low	R/W	3B5	3D5	OF
Vertical Retrace Start	W	3B5	3D5	10
Vertical Retrace End	W	3B5	3D5	11
Vertical Display Enable End	R/W	3B5	3D5	12
Offset	R/W	3B5	3D5	13
Underline Location	R/W	3B5	3D5	14
Start Vertical Blanking	R/W	3B5	3D5	15
End Vertical Blanking	R/W	3B5	3D5	16
CRTC Mode Control	R/W	3B5	3D5	17
Line Comparator Register	R/W	3B5	3D5	18
Read-back CRT Latches	R	3B5	3D5	22
Attribute Index Toggle	R	3B5	3D5	24
Attribute Index Register	R/W	3B5	3D5	23

GENERAL REGISTERS

MISCELLANEOUS OUTPUT REGISTER

Read address = 3CC hex; Write address 3C2 hex

Bit Description

0 Input/Output Address Select -This bit maps the CRTC I/O addresses for monochrome or color emulation.

0 = Monochrome emulation with CRTC addresses set to 3Bx hex, Input Status 1 register set to 3BA hex.
1 = Color emulation with CRTC addresses set to 3Dx, Input Status 1 register set to 3DA hex.

1 Enable RAM
0 = Disable Video RAM address decode from the system microprocessor.

1 = Enable Video RAM to the system microprocessor.

2,3 Clock Select - These two bits, CSEL0 and CSEL1, are used with 3DF index D bit 5 as follows:

CS2	CS1	CS0	Clock
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	65 MHz
0	1	1	44.9 MHz
1	0	0	14.161 MHz (derived from 28.322)
1	0	1	18 MHz (derived from 36 MHz)
1	1	0	40 MHz
1	1	1	36 MHz

(These bits have been overridden by the Oak Extended Register 06. Any bits written here must be the same as those written to Extended Register 06).

4 Reserved

5 Page Bit For Odd/Even - Select between two pages of memory when in the odd or even modes (0-5).

0 - Low 64K page of memory

1 - High 64K page of memory

6 Horizontal Sync Polarity

0 - Positive Vertical Retrace

1 - Negative Vertical Retrace

7 Vertical Sync Polarity

0- Positive Vertical Retrace

1- Negative Vertical Retrace

Bits 6 and 7 are used to select the vertical size of the monitor as follows:

Bit7	Bit6	
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

INPUT STATUS REGISTER 0

Read address = 3C2 hex

Bit	Description
0-3	Reserved

4 Switch Sense Bit • Reports the status of one of the four switches selected via the clock select to the Miscellaneous Output register. This bit allows the power-on initialization to determine if a monochrome or color monitor Is connected to the system.

0 - Selected sense switch is off or 0.
1 - Selected sense switch is on or 1.

5,6 Reserved

7 CRT interrupt

0 = Vertical retrace interrupt is pending
1 = Vertical retrace Interrupt is cleared.

INPUT STATUS REGISTER 1

Read address = 3BA/3DA hex

Bit Description

0 Display Enable = Monitors the status of the display. To avoid glitches on the display, some programs watch this bit to restrict screen updates to inactive display periods. The VGA has been designed to eliminate this requirement, so display screen updates may be made at any time.

0 - The display of video data is enabled.

1 - The display is in horizontal or vertical retrace mode.

1,2 Reserved

3 Vertical Retrace

0 - Video information Is being displayed.

1 - A vertical retrace interval is in progress.

4,5 Diagnostic Usage - reports the status of two of the VGA attribute controller outputs. The values set Into the Video status MUX field of the Color Plans Enable register determine which colors are input to these two diagnostic bits.

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

6,7 Reserved

FEATURE CONTROL REGISTER

Read address = 3CA hex; Write address = 3BA/3DA hex

Bit	Description
0-2	Reserved
3	Vertical Sync Select 0 - This bit should always be set to 0 to enable normal Vertical Sync output to the monitor 1 - The Vertical Sync output is the logical OR of vertical Sync end Vertical display enable.
4-7	Reserved

DAC REGISTERS

PEL Mask	R/W	3C6
DAC State Register	R	3C7
PEL Address (Read Mode)	W	3C7
PEL Address (Write Mode)	R/W	3C8
PEL Data Register	R/W	3C9

SEQUENCER REGISTERS

SEQUENCER ADDRESS REGISTER

Port address - 3C4 hex

This register is a pointer register located at address 03C4 hex. It is loaded with a binary value that points to the SEQUENCER Data register where data is to be written. This value is referred to as the Index.

Bit	Description
0-2	Sequencer Address bits - A binary value pointing to the register where data is to be read or written.
3-7	Reserved

RESET REGISTER

Port address = 3C5 hex, Index 00 hex

This Is a read/write register pointed to when the value in the Sequencer Address register is 00 hex.

Bit	Description
0	Asynchronous Reset - This bit, synchronous reset, or both should be set to O before changing bit 0 or bit 3 of the Clocking Mode register or bit 2 or bit 3 of the Miscellaneous Output register, or all bits of register 3DF index D. 0 - Asynchronous clear and halt the sequencer. This may cause data loss In the dynamic RAM's. 1 - Bit 1 and 0 must be 1 to allow the sequencer to operate.
1	Synchronous Reset This bit, asynchronous reset, or both should be set to 0 before changing bit 0 or bit 3 of the Clocking Mode register or bit 2 or bit 3 of the Miscellaneous Output register, or all bits of register 3DF index D. 0 - Synchronous clear and halt the sequencer.

1 - Bit 1 and 0 must be 1 to allow the sequencer to operate.

2-7 Reserved

CLOCKING MODE REGISTER

Port address = 03C5 hex; Index 01 hex

This is a read/write register pointed to when the value in the Sequencer Address register is 01 hex.

Bit	Description
0	8/9 Dot Clocks • The 9 dot mode Is for Alphanumeric modes only. The ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also see the Line Graphics Character Code bit in the Attribute Mode Control register section. 0 - Directs the sequencer to generate nine dot wide character clocks. 1 - Generate eight dot wide character clocks.
1	Reserved
2	Shift Load 0 - If bit 4 Is set to 0, also, the video serializers are reloaded every character clock. 1 - The video serializers are reloaded every other character clock. this mode is useful when 16 bits are fetched per cycle and chained together In the shift load registers.
3	Dot clock - All other timings will be affected since they are derived from the dot dock. 0 - Select normal dot docks derived from the sequencer master clock Input. 1 - The master clock will be divided by 2 to generate the dot clock. This is used for 320 and 360 horizontal PEL modes.

4 Shift 4

0 - The video serializers are reloaded every character clock.
1 - The serializers are loaded every fourth character clock This is useful when 32 bits are fetched per cycle and chained together in the shift registers.

5 Screen Off - This bit is used for fast full-screen updates.

0 = Normal screen operation.
1 = Turns off the video screen and assigns the maximum memory bandwidth to the system CPU.

6,7 Reserved

MAP MASK REGISTER

Port address = 3C5 hex; index 02 hex

This is a read/write register pointed to when the Sequencer Address register is 02 hex.

Bit	Description
0-3	Map Mask - For odd/even modes, maps 0 and 1, and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation.

0 = Disable memory write to the corresponding map.

1 = Enables the system to write to the corresponding map. If all four bits are set to 1, the system CPU can perform a 32-bit operation with only one memory cycle.

4-7 Reserved

CHARACTER MAP SELECT REGISTER

Port address = 3C5 hex; index 03 hex

This is a read/write register pointed to when the value in the Sequencer Address register is 03 hex.

Bit	Description
0,1	Character Map Select B - Selects the portion of map 2 used to generate Alpha characters with bit 4 as the high bit when attribute bit 3 is 0.

Bit4	Bit1	Bit0	Map	Table location
0	0	0	0	1st 8k of Map 2
0	0	1	1	3rd 8k of Map 2
0	1	0	2	5th 8k of Map 2
0	1	1	3	7th 8k of Map 2
1	0	0	4	2nd 8k of Map 2
1	0	1	5	4th 8k of Map 2
1	1	0	6	6th 8k of Map 2
1	1	1	7	8th 8k of Map 2

2,3 Character Map Select A - Select the portion of map 2 used to generate Alpha characters with bit 5 as the high bit when attribute bit 3 is 1. Bit 3 of the attribute byte normally controls the ON/OFF of the foreground intensity in text modes. This bit may be redefined as a switch between character sets. For this feature to be enabled, the following statements must be true:

* The setting value of Character Map Select A does not equal the value of Character Map Select B.

* The Memory Mode register bit 1, must be equal to 1.

If either of these are not true, the first 16K of Map 2 is used.

Bit5	Bit3	Bit2	Map	Table Location
0	0	0	0	1st 8k of Map 2
0	0	1	1	3rd 8k of Map 2
0	1	0	2	5th 8k of Map 2
0	1	1	3	7th 8k of Map 2
1	0	0	4	2nd 8k of Map 2
1	0	1	5	4th 8k of Map 2
1	1	0	6	6th 8k of Map 2

	1	1	1	7	8th 8k of Map 2

4 Character Map Select High Bit B
5 Character Map Select High Bit A
6,7 Reserved

MEMORY MODE REGISTER

Port address = 3C5 hex; index 04 hex

This is a read/write register pointed to when the value in the Sequencer Address register is 04 hex

Bit Description

0 Reserved

1 Extended memory
- 0 = No extended memory present. Display memory is less than 64 Kbytes.
- 1 = Extended memory is present. Display memory is greater than 64 Kbytes. If set to 1 the VGA is configured to use 256k bytes of video memory. This also enables character map selection.

2 Odd/Even
- 0 = Directs even CPU addresses to access maps 0 and 2, and odd CPU addresses to access maps 1 and 3.
- 1 = If bit 3 is set to 0, this bit causes system CPU addresses to sequentially address data within a bit map.

3 Chain 4
- 0 = If bit 2 is set to 1, this bit enables the system CPU to address data sequentially within a bit map by use of the Map Mask register.
- 1 = Causes two low-order address bits to select the map that will be accessed as follows:

A1	A0	Map Selected
0	0	0
0	1	1
1	0	2
1	1	3

4-7 Reserved

CRT CONTROLLER REGISTERS

CRT CONTROLLER ADDRESS REGISTER

Port address = 3B4/3D4 hex

This register is a pointer register located at 3B4 hex for Monochrome emulation modes or 3D4 hex for Color emulation modes depending on bit 0 of the Miscellaneous output register at address 3C2 hex. The CRT Controller Addresses register is loaded with a binary value, or index, that points to the CRT Controller Data register where data is to be Written. All CRT controller registers are read/write registers.

Bit	Description
0-4	CRT Controller Address Bits - A binary value programmed in these bits selects one of the CRT Controller registers where data is to accessed.
5	Test Bit - Must remain 0.
6,7	Reserved

HORIZONTAL TOTAL REGISTER

Port address = 3B5/3D5 hex; index = 00 hex

Bit	Description
0-7	Horizontal Total This register defines the total number of characters in the horizontal interval including the retrace time. This value directly controls the period of the horizontal retrace output signal. Character clock inputs to the CRT controller and counted by an international horizontal character counter. This value is compared with the horizontal character values to provide horizontal timings. All horizontal and vertical timings are based upon the horizontal register. The value programmed is 5 less than the desired value.

HORIZONTAL DISPLAY ENABLE END REGISTER

Port address = 3B5/3D5 hex; index = 01 hex

Bit	Description
0-7	Horizontal Display Enable End - The total number of displayed characters minus 1. This register defines the length of the horizontal display enable signal. It determines the number of displayed characters per horizontal line.

START HORIZONTAL BLANKING REGISTER

Port address = 3B5/3D5 hex; index = 02 hex

Bit	Description
0-7	Start horizontal blanking - Determines when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

END HORIZONTAL BLANKING REGISTER

Port address = 3B5/3D5 hex; index = 03 hex

This register determines when the horizontal blanking output signal becomes inactive.

Bit	Description
0-4	End Horizontal Blanking - The horizontal blanking signal width is determined as follows: Value of Start Blanking register + width of blanking signal in character clock units =6-bit result to be programmed into the End Horizontal blanking register. Bit number 5 is located in the End Horizontal Retrace register. If these six bits equal the six least significant bits the horizontal character counter, the horizontal blanking signal becomes inactive.
5,6	Display Enable Skew Control - These two bits indicate the magnitude of display enable skew. Bits 5 and 6 and the amount of skew are as follows:

Bit6	Bit5	Skew
0	0	Zero character clock skew
0	1	One character clock skew
1	0	Two character clock skew
1	1	Three character clock skew

7 Test Bit - Must be set to 1

START HORIZONTAL RETRACE PULSE REGISTER

Port address = 3B5/3D5 hex; index = 05 hex

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

Bit	Description
0-4	End horizontal Retrace - The value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive (logical 0). To calculate the width of the retrace signal use the following algorithm: Value of Start Horizontal Retrace register + width of Horizontal Retrace signal in character in clock units = 5-bit result to be programmed into the End Horizontal Retrace register.

PRESET ROW SCAN REGISTER

Port address = 3B5/3D5 hex; index = 08 hex

Bit	Description
0-4	Preset Row Scan (PEL Scrolling) - These bits specify the starting row scan counter after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the scan is cleared (not preset).
5,6	Byte Panning Control - This field controls byte panning in modes programmed as multiple shift modes, which is required for PEL-panning operations. The Horizontal PEL Panning register in the Attribute Controller provides panning of up to 8 individual PEL-panning operations. In single byte shift modes, the CRT Controller start address is incremented and attribute panning is reset to 0 to pan to the next higher PEL. In multiple shift modes, the byte pan bits are used as extensions to the attribute PEL Panning register. This allows panning across the width of the video output shift.
7	Reserved