Databook

Local Bus VGA Graphics Controller

OTI-087

NEW

OAK TECHNOLOGY, INC.™

System Solutions in Silicon

OTI-087X Addendum to the Databook

This Addendum describes changes to the OTI-087 February 1993 databook for OTI-087X parts. The OTI-087X currently does not support the RAS only refresh DRAM, 260's type DRAM and integrated feature connector support.

Page	Description
1	Disregard the reference to RAS only refresh in the feature list. This is currently not supported.
8	Disregard CAS0n, CAS1n, CAS2n and CAS3n signals on the Operational Block Diagram.
13	This MD interface is not supported with this OTI-087 revision.
16	Disregard CAS0n, CAS1n, CAS2n and CAS3n signals on the Memory Mapping Configuration.
25	EPDATA should be DCn under the OTI-087 (LB386/486) column.
28	Pin 99 on OTI-087 (LB 386/486) should be DCn.
37	Extended Register 8, bits 6, 1, 0 should be as below. Also, pin 99 does not apply.

Bits 6, 1, 0	Pin 19	Pin 20
1 0 1	EPCLK	EPDATA
110	EPCLK	EPDATA

Bit 7	Reserved.

60	See attached for new Local Bus Schematics.

Preface

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OTI-087 LOCAL BUS VGA CONTROLLER

Description

The OTI-087 is a highly integrated, single chip Local Bus VGA Controller compatible with the IBM VGA standard. The OTI-087 offers a low-cost implementation for 24-bit color at a resolution of 640x480 while being capable of high resolutions including 1024x768 non-interlaced with 256 colors and 1280x1024 interlaced with 256 colors. The OTI-087 is completely compatible with the IBM VGA standard and implements all registers and data paths while providing improved performance and additional functionality. Especially attractive for motherboard applications, the OTI-087 supports high speed local bus implementations for cost-effective high performance graphics.

Features

- IBM VGA compatible graphics controller with resolutions up to:
  - 1024x768, 256 colors Non-Interlaced
  - 1280x1024, 256 colors Interlaced
  - 640x480, 16.8 million colors (24-bit)
- 100% Hardware and BIOS compatible with IBM's VGA
- Supports up to 2 MBytes of memory:
  - 2, 4 or 8 64K X 16 DRAMs
  - 2, 4, 8 or 16 256K X 4 DRAMs
  - 2 or 4 256K X 16 DRAMs
  - 2 or 4 512K X 8 DRAMs
- Hardware cursor (64x64 2 bits/pixel)
- Integrated feature connector support
- Write cache for high speed local bus implementation
- Read cache optimizes memory bandwidth usage
- Integrated zero wait state AT bus performance
- Supports 8, 16, or 32-bit memory interface with fast page operation
- Supports CAS before RAS and RAS only refresh
- Supports VESA-standard high vertical refresh rates of 72 Hz for flicker-free displays
- Up to 80 MHz maximum video clock rate
- Complete linear addressability in protected mode
- Packed pixel format for 256 color modes
- Foreground/background color expansion registers for fast text output
- 16-bit graphics latch for true 16-bit operations in planar modes
- Special 256 color pattern and fill modes increase performance
- Supports 132 column text
- Integrated bus interface for PC/XT/AT and local bus implementations
- Supports portrait monitors
- True 16-bit I/O read/write operations
- EEPROM support provides switchless configurations

Supported Screen Formats

The OTI-087 not only supports all standard IBM VGA modes, but the following extended modes as well.

Mode	Resolution	Colors	Font	Alpha Format	Dot Clk(MHz)	H-freq(KHz)	V-freq(Hz)	Non-Interlaced	Video Memory	VESA
12h*	640 x 480	16	8 x 16	80 x 30	25.175	31.50	60	Yes	256K	N/A
12h	640 x 480	16	8 x 16	80 x 30	31.500	37.86	72	Yes	256K	Standard
4Eh*	80 x 60	16	8 x 8	80 x 60	25.175	31.50	60	Yes	256K	N/A
4Fh*	132 x 60	16	8 x 8	132 x 60	40.000	31.50	60	Yes	256K	N/A
50h*	132 x 25	16	8 x 14	132 x 25	40.000	31.50	70	Yes	256K	N/A
51h*	132 x 43	16	8 x 8	132 x 43	40.000	31.50	70	Yes	256K	N/A
52h*	800 x 600	16	8 x 16	100 x 37.5	36.000	35.16	56	Yes	256K	Mfg. G.L.
52h	800 x 600	16	8 x 16	100 x 37.5	40.000	37.88	60	Yes	256K	Mfg. G.L.
52h	800 x 600	16	8 x 16	100 x 37.5	50.000	48.08	72	Yes	256K	Standard
53h*	640 x 480	256	8 x 16	80 x 30	25.175	31.50	60	Yes	512K	N/A
53h	640 x 480	256	8 x 16	80 x 30	31.500	37.86	72	Yes	512K	Standard
54h*	800 x 600	256	8 x 16	100 x 37.5	36.000	35.16	56	Yes	512K	Mfg. G.L.
54h	800 x 600	256	8 x 16	100 x 37.5	40.000	37.88	60	Yes	512K	Mfg. G.L.
54h	800 x 600	256	8 x 16	100 x 37.5	50.000	48.08	72	Yes	512K	Standard
55h	1024 x 768	4	8 x 16	128 x 48	44.900	35.52	87	No	256K	N/A
55h*	1024 x 768	4	8 x 16	128 x 48	65.000	48.36	60	Yes	256K	Mfg. G.L.
55h	1024 x 768	4	8 x 16	128 x 48	78.000	56.69	70	Yes	256K	Standard
55h	1024 x 768	4	8 x 16	128 x 48	78.000	58.04	72	Yes	256K	N/A
56h	1024 x 768	16	8 x 16	128 x 48	44.900	35.52	87	No	512K	N/A
56h*	1024 x 768	16	8 x 16	128 x 48	65.000	48.36	60	Yes	512K	Mfg. G.L.
56h	1024 x 768	16	8 x 16	128 x 48	78.000	56.69	70	Yes	512K	Standard
56h	1024 x 768	16	8 x 16	128 x 48	78.000	58.04	72	Yes	512K	N/A
57h	768 x 1024	16	8 x 16	96 x 64	44.900	46.77	87	No	512K	N/A
57h*	768 x 1024	16	8 x 16	96 x 64	65.000	59.74	55	Yes	512K	N/A
58h*	1280 x 1024	16	8 x 16	160 x 64	78.000	48.75	87	No	1M	N/A
59h[2]	1024 x 768	256	8 x 16	128 x 48	44.900	35.52	87	No	1M	N/A
59h*[1]	1024 x 768	256	8 x 16	128 x 48	65.000	48.36	60	Yes	1M	Mfg. G.L.
59h[1]	1024 x 768	256	8 x 16	128 x 48	78.000	56.69	70	Yes	1M	Standard
59h[1]	1024 x 768	256	8 x 16	128 x 48	78.000	58.04	72	Yes	1M	N/A
5Ah*[2]	640 x 480	64K	8 x 16	80 x 30	50.000	31.50	60	Yes	1M	N/A
5Ah[1]	640 x 480	64K	8 x 16	80 x 30	63.000	37.86	72	Yes	1M	Standard
5Bh*	640 x 400	32K/64K	8 x 16	80 x 25	50.000	31.50	70	Yes	512K	N/A
5Ch*[2]	640 x 480	32K	8 x 16	80 x 30	50.000	31.50	60	Yes	1M	N/A
5Ch[1]	640 x 480	32K	8 x 16	80 x 30	63.000	37.86	72	Yes	1M	Standard
5Dh*[1]	800 x 600	32K	8 x 16	100 x 37.5	78.000	37.50	60	Yes	1M	Mfg. G.L.
5Eh*	1280 x 1024	256	8 x 16	160 x 64	78.000	48.75	87	No	2M	N/A
5Fh*	640 x 480	16.8M	8 x 16	80 x 30	78.000	31.55	60	Yes	1M	N/A
60h*[1]	800 x 600	64K	8 x 16	100 x 37.5	78.000	37.50	60	Yes	1M	Mfg. G.L.
61h*	640 x 400	256	8 x 16	80 x 25	25.175	31.50	70	Yes	256K	N/A

Software Driver Support

Oak Technology was the first graphics company to promote the importance of the hardware-software driver relationship. Thus, Oak is committed to providing customers with the most powerful software drivers. Oak's software driver support includes the fastest drivers available for popular applications including:

AutoCAD
AutoShade
CADvance
GEM
Lotus 1-2-3/Symphony
P-CAD
OS/2
OS/2 Presentation Manager
VersaCAD
VESA BIOS Extensions
WordPerfect/DrawPerfect/PlanPerfect
Ventura
UNIX (ISC & SCO)
OrCAD
EasyCAD/FastCAD
Microsoft Windows
Wordstar

Display Memory Interface

The OTI-087 supports 64Kx16, 256Kx4, 256Kx16, and 512Kx8 DRAM devices. The OTI-087 provides all the necessary control signals and address and data lines to access the video memory in page mode. The control signals can be programmed to optimize memory cycles for a given memory type and speed for a specific memory clock. The maximum video buffer size is 2Mbytes when used with 256Kx4, 256Kx16 or 512Kx8 DRAMs and 1Mbyte when used with 64Kx16 DRAMs. Minimum configuration is 256Kbytes when used with 64Kx16 or 256Kx4 DRAMs and 1Mbyte when used with 512Kx8 or 256Kx16 DRAM. The video buffer can be addressed through either a programmable linear address range above 1M or through the conventional video address (A0000 to $BFFFF_H$) using the segment registers.

Clock Interface

Up to 16 external video clock frequencies can be selected by four programmable clock select pins. Video clock frequencies up to 80 MHz can be supported. When implemented with the OTI-068 Dual Clock Generator, the OTI-087 can select sixteen pixel clock frequencies providing support for both conventional and flicker-free VESA vertical refresh rates without any hardware switches. The OTI-068 also supports three memory clock frequencies which can be selected through hardware configuration to optimize performance with a wide variety of DRAM types and speeds.

System Bus Interface

The system bus of the OTI-087 can be connected to the PC system in three different configurations: on-board local bus, add-on local bus and on-board AT bus. The OTI-087 can also be connected to the AT bus. The mode of operation is defined by the **Configuration Register 1** status, set through the MD[7:0] bus during reset time.

System Configuration	Bit 2	Bit1
Local Bus	0	0
Local Bus Add-on	0	1
On-board AT	1	0
Add-on AT	1	1

Local Bus Interface

In Local Bus configuration, the OTI-087 can interface to the 80286, 80386SX, 80386DX, and 80486 CPUs. Configuration of the OTI-087 for the proper CPU local bus is accomplished through the ADSn pin and the **Configuration Register 2** as detailed in the table below. **Configuration Register 2** is set through the MD[15:8] bus during reset.

Local Bus Mode	ADSn	Bit 1	Bit 0
80286 Local Bus	0	0	0
80386SX Local Bus	1	0	0
80386DX Local Bus	1	0	1
80486 Local Bus	1	1	0

To ensure the above detection scheme will operate properly, a weak pull-down resistor should be connected to the ADSn pin of the OTI-087. Since the 80286 processor does not have ADSn, this signal should remain low during reset in 80286 designs. For proper operation in 80386 and 80486 processor designs, this signal will be reset high.

OTI-087 Local Bus with 80286 and 80386SX Processors

The local bus interface of the OTI-087 provides an optimal implementation for 80286 and 80386SX designs which use Oak Technology's OTI-020 system chipset. An implementation of the OTI-087 with the OTI-020 requires no external logic for local bus interface.

The video space of the OTI-087/OTI-020 local bus video system is defined by the VIDEO1 register (port $1F_H$ index 5). When any one of the video segments in this register is enabled, the OTI-020 system chipset generates a video cycle to the external bus and terminates the CPU cycle. If the video segments are disabled, the local bus OTI-087 will terminate the CPU cycle. Graphics Register $3DF_H$, Index 6 only affects the access to video memory and has no effect on the generation of SRDY. At system boot-up time, the system will scan for the presence of any off-board memory which occupies the A0000~$BFFFF_H$ range. If off-board video memory is detected, the VIDEO1 register (present in both the OTI-020 system chipset and the OTI-087) will be programmed so that the local bus system responds to all the memory in A0000~$BFFFF_H$, excluding the enabled segments in the VIDEO1 register.

The OTI-087 supports 16-bit, zero-wait-state CPU memory operations through the CPU local bus. The OTI-087 uniquely employs both a read cache and a write cache to achieve zero-wait-state memory operations for local bus speeds up to 33 MHz. During the CPU memory cycle, the OTI-087 interprets the status lines (WRn and DCn) and the address CA19~CA17 (101_H) gated with the VIDEO1 register to generate a local bus memory cycle. If the requested data is already inside the OTI-087 read cache during a memory read, SRDY is returned in the next CPU clock, thus a zero-wait-state memory cycle. Otherwise, SRDY is not returned until the data is read from the video memory and driven out to the bus. For writes to video memory, a memory write request is stored inside the write cache and SRDY is returned in the next CPU clock for a zero-wait-state memory cycle. If either the write cache is full or the write address does not share the same cache page as the previous write, then SRDY is not returned until the data is actually written to the video memory.

The OTI-087 supports 16-bit I/O access and 8-bit memory access for DMA and MASTER cycles. During a DMA or MASTER cycle, the OTI-087 receives I/O and memory commands from the AT-bus and transfers data to the local SD bus as if it were a 16-bit device. In this case, both SD[7:0] and SD[15:8] are driven with the same data. During I/O cycles, the OTI-087 receives commands from the AT-bus and transfers data on the local bus. The system chipset is responsible for routing the address and data to and from the AT-bus.

80386DX and 80486 Local Bus

This section refers to the 80386DX/80486 block diagrams following this section. The OTI-087 requires four buffers (A,B,E,F in the diagram) and 1 PAL to interface with the 80386DX CPU. Two additional buffers (C,D in the diagram) are required to interface with the 80486 CPU. The PAL is used to decode the upper address of the CPU and generate the CPU address 0,1 and the CPUBHEn signal for the OTI-087. The A,B buffers are used to interface the OTI-087 data bus to AT-data bus while the C,D,E,F buffers are used to interface the OTI-087 data bus to the CPU data bus.

During I/O, DMA or MASTER cycles, the OTI-087 receives bus commands from the AT-bus. During a CPU memory cycle, the OTI-087 will use the CPUA0/A1/BHEn signals to execute the cycle. The LBSELn signal is the protocol between the system chipset and the OTI-087 to determine ownership of the current memory cycle. If the current memory cycle belongs to the OTI-087 address space, the OTI-087 forces the LBSELn signal low at the beginning of T2 and terminates the cycle with SRDY. If the current memory cycle does not belong to the OTI-087 address space the system chipset should terminate the cycle. In 80386DX and 80486 configura-

tions, there are two reset signals connected to the OTI-087. The RSET signal is connected to the system reset and the CPURESET is connect to the CPU reset. The OTI-087 uses the CPURESET signal to synchronize the internal clock and uses the RSET signal to reset the OTI-087. If the system chipset does not drive a valid address to the CPU bus during DMA or MASTER cycles, then more buffers are necessary to route the address to the CPU bus. Buffer G in 80386DX/80486 block diagrams illustrate this implementation.

Summary of Performance Features

The OTI-087 implements all of the standard state-of-the-art features for high speed frame-buffer graphics controllers. These standard features include independent memory and pixel clocks, support for high refresh displays, highly integrated bus interfaces, and true 16-bit I/O read/write operations. In addition, the OTI-087 implements several next generation features which advance the state-of-the-art in graphics frame-buffer technology.

High Speed Local Bus

The OTI-087 is one of the first PC graphics controllers designed from the ground up for motherboard architectures implementing direct CPU interfaces to the video controller. The local control signals of the OTI-087 provide accelerated system to video memory transfers. Timing overhead is also reduced. To take advantage of the high transfer rates, the OTI-087 implements the most features of any frame-buffer controller for assisting CPU-based graphics operations.

Hardware Cursor

The Hardware Cursor (HC) increases the overall graphics performance by reducing the need for the CPU to redraw the cursor during each update. Also, the image under the cursor does not have to be updated by software when the cursor is moved. Lastly, the cursor appears continuously and is more responsive.

Write Cache

When writing to the OTI-087, both data and address are latched from the system bus and the zero-wait-state signal is activated, unless the cache is full. When implemented in the AT-bus configuration, the OTI-087 will exhibit zero-wait-state performance in lower resolution/color and planar modes. In higher resolution, the percentage of zero-wait cycles will decrease for packed pixel modes with increasing bus speed, resolution, color depth, and vertical refresh.

Read Cache

The read cache of the OTI-087 was designed to accelerate bitblt functions. When executing block moves, often the next operation requires a read from an adjacent memory location. In this case, the desired data will be in the read cache and the operation can execute without waiting for a memory cycle.

Linear Addressability

In extended video modes where more than 256Kbytes of video buffer are required, the video driver must perform segment checking and address calculation to determine a given pixel's location in video memory. At programmable addresses above 1 Mbyte, the OTI-087 provides linear memory mapping thereby eliminating segment checking. Linear addressing speeds all functions when running applications in protected-mode.

Foreground/Background Color Expansion

In packed pixel modes, the output of simple text becomes more cumbersome. To reduce the number of individual memory operations required, the OTI-087 contains foreground/background color expansion registers which allow eight consecutive bytes to be expanded from one byte containing the foreground or background bits. A pixel masking capability is also implemented to be able to leave specified pixels unchanged. This also speeds masked bitblt functions.

256 Color Patterns and Fills

For packed pixel modes, the OTI-087 provides a pattern register for defining patterns and expanding the color information from either OTI-087 registers or CPU data. This allows fast pattern fill.

16-bit Graphics Latch

Most currently available VGA controllers only allow for byte operations in many cases. The OTI-087, as with previous generations of Oak VGA controllers, provides true 16-bit move operations in all situations. Relative to other VGA controllers, this is particularly useful for pattern blts and source copy bitblts where MOVSW instructions can replace MOVSB instructions.

EEPROM Support

In a VGA-based video system, certain configuration information must be available to the video BIOS. It is common practice on many video adapter boards to use jumpers or switches to provide the proper settings. These switch settings can cause confusion for the consumer. To simplify the situation, the OTI-087 provides support for a serial EEPROM which stores the specific configuration information. The configuration is done through software, eliminating all jumpers and switches.

80 Mbyte/sec Video

Fixed clock rates to 80 MHz allow the OTI-087 to offer vertical refresh rates at 1024x768 that exceed the VESA standard of 70 Hz for high vertical refresh displays. Depending on the capabilities of the monitor, the OTI-087 can support up to 1024x768 with 256 colors at a 76 Hz vertical screen refresh.

OTI-087 System Block Diagram